CONN-MGT-ILT (v1.0)

# **Course Description**

Learn how to employ serial transceivers in your 7 series FPGA design. Understand and utilize the features of the serial transceiver blocks, such as 8B/10B and 64B/66B encoding, channel bonding, clock correction, and comma detection. Additional topics include use of the 7 Series FPGAs Transceiver Wizard, synthesis and implementation considerations, board design as it relates to the transceivers, and test and debugging. This course combines lectures with practical hands-on labs.

## Level – Connectivity 3

Course Duration – 3 days

#### Course Part Number - CONN-MGT-ILT

Who Should Attend? – FPGA designers and logic designers

- Prerequisites
- Verilog or VHDL experience (or the Designing with Verilog or the Designing with VHDL course)
- Familiarity with logic design (state machines and synchronous design)
- Basic knowledge of FPGA architecture and Xilinx implementation tools is helpful
- Familiarity with serial I/O basics and high-speed serial I/O standards is also helpful

### Software Tools

- Vivado® System Edition 2015.1
- Mentor Graphics QuestaSim simulator 10.3d

### Hardware

- Architecture: 7 series FPGAs\*
- Demo board: Kintex®-7 FPGA KC705 board\*

\* This course focuses on the Kintex-7 architecture. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe and utilize the ports and attributes of the serial transceivers in the 7 series FPGAs
  - Effectively utilize the following features of the gigabit transceivers:
  - 8B/10B and other encoding/decoding, comma detection, clock correction, and channel bonding
  - Pre-emphasis and linear equalization
- Use the 7 Series FPGAs Transceivers Wizard to instantiate GT primitives in a design
- Access appropriate reference material for board design issues involving the power supply, reference clocking, and trace design

## **Course Outline**

## Day 1

- 7 Series FPGAs Overview
- 7 Series FPGAs Transceivers Overview
- 7 Series FPGAs Transceivers Clocking and Resets
- 8B/10B Encoder and Decoder
- Lab 1: 8B/10B Encoding and Bypass
- Commas and Deserializer Alignment
- Lab 2: Commas and Data Alignment

#### Day 2

- RX Elastic Buffer and Clock Correction
- Lab 3: Clock Correction
- Channel Bonding
- Lab 4: Channel Bonding

# Designing with Multi-Gigabit Serial I/O

## **Connectivity 3**

## **Course Specification**

- Transceiver Wizard Overview
- Lab 5: Transceiver Core Generation
- Transceiver Simulation
- Lab 6: Simulation
- Transceiver Implementation
- Lab 7: Implementation
- Physical Media Attachments

#### Day 3

- 64B/66B Encoding and the Gearbox
- Lab 8: 64B/66B Encoding
- Transceiver Board Design Considerations
- Transceiver Test and Debugging
- Lab 9: Transceiver Debugging
- Lab 10: IBERT Lab or
- Lab 11: System Lab
- Transceiver Application Examples

# Lab Descriptions

- Lab 1: 8B/10B Encoding and Bypass Utilize the 8B/10B encoder and decoder and observe running disparity. Learn how to bypass the 8B/10B encoder and decoder.
- Lab 2: Commas and Data Alignment Use programmable comma detection to align a serial data stream.
- Lab 3: Clock Correction Utilize the attributes and ports associated with clock correction to compensate for frequency differences in the TX and RX clocks.
- Lab 4: Channel Bonding Modify a design to use two transceivers bonded together to form one virtual channel.
- Lab 5: Transceiver Core Generation Use the 7 Series FPGAs Transceivers Wizard to create instantiation templates.
- Lab 6: Simulation Simulate the transceiver IP using the IP example design.
- Lab 7: Implementation Implement the transceiver IP using the IP example design.
- Lab 8: 64B/66B Encoding Generate a 64B/66B transceiver core by using the 7 Series FPGAs Transceivers Wizard, simulate the design, and analyze the results.
- Lab 9: Transceiver Debugging Debug the transceiver IP using the IP example design and Vivado debug cores.
- Lab 10: IBERT Create an IBERT design to verify physical links.
- Lab 11: System Perform all design steps from planning the design, generating the core, integrating the core into a design, simulating, implementing and debugging the design, and optimizing the link parameter using an evaluation board.

# **Register Today**

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# **Designing with Multi-Gigabit Serial I/O**

Connectivity 3

CONN-MGT-ILT (v1.0)

Course Specification

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